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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,217	ZIMMERMAN ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication..
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered July 05, 2006.

- Claims 1-29 are pending. Claims 10, 11, 16, 18 & 25 are amended.
- Claims 30 & 31 are added.

Response to Amendment

Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-7, 10, 12-15, & 30-31 are rejected under 35 U.S.C. 102(b) as being unpatentable over Kaneko et al. US Pat no. 5,561,672.

As per claim 1, 30 & 31:

Kaneko teaches an electronic system and method comprising: a first memory module having a first memory array (Figure 1A # 15) and a first buffer logic coupled to the first memory array (Figure 1A # 41); and a second memory module having a second memory array (Figure 1B # 9) and a second buffer logic coupled to the second memory array (Figure 1B # 21), and transmits a test pattern to the first memory module to carry out a test of the first memory module independently of the memory controller (column 2, lines 25-60).

As per claim 2:

Kaneko teaches an electronic system as rejected in claim 1 above further comprising: a memory controller coupled to the second buffer logic (Figure 1B # 22); and a processor (Figure 1B # 25) coupled to the memory controller to execute instructions stored in the second memory array of the second memory module under the control of the memory controller.

As per claim 3:

Kaneko teaches an electronic system as rejected in claim 2 above, wherein the memory controller transmits a command to the second buffer logic under the control of the processor to cause the second buffer logic to carry out a test of the first memory module (Figure # 4A).

As per claim 4:

Kaneko teaches an electronic system as rejected in claim 3 above, further comprising a memory bus coupling together the memory controller, the first memory module and the second memory module, and wherein the test pattern is transmitted across the memory bus (Figure 1A # 17).

As per claim 5:

Kaneko teaches an electronic system as rejected in claim 1 above, further comprising a point-to-point bus coupling the second buffer logic of the second memory module to the first buffer logic of the first memory module, wherein the test pattern is transmitted by the second buffer logic across the point-to-point bus to the first buffer logic (Figure 1 # 17).

As per claim 6:

Kaneko teaches an electronic system as rejected in claim 1 above, further comprising a test source coupled to the second buffer logic (Figure 4A), wherein the test source transmits a command to the second buffer logic to cause the second buffer logic to carry out a test of the first memory module (Figure 4A).

As per claim 7:

Kaneko teaches an electronic system as rejected in claim 6 above, further comprising a serial bus coupling the second buffer logic to the test source (Figure 4A # 300), wherein the command is transmitted by the test source across the serial bus to the second buffer logic.

As per claim 10:

Kaneko teaches the electronic system as rejected in claim 1 above, wherein the test pattern incorporates commands for the first buffer logic to carry out (Figure 4A # 314).

As per claim 12:

Kaneko teaches the electronic system as rejected in claim 1 above, further comprising an analysis module having a third buffer logic having an interface to couple the third buffer logic to an analysis device, wherein the analysis module is interposed between the second buffer logic and the first buffer logic such that the second buffer logic is coupled to the third buffer logic and the third buffer logic is coupled to the first buffer logic, and the test pattern transmitted by the second buffer logic to the first buffer logic passes through the third buffer logic (Figure 4A # 13, column 5, lines 5-65).

As per claim 13:

Kaneko teaches the electronic system as rejected in claim 12 above, further comprising: a first point-to-point bus coupling the first buffer logic of the first memory module to the third buffer logic (Figure 4A-B); and a second point-to-point bus coupling the second buffer logic of the second memory module to the third buffer logic (Figure 4A-B).

As per claim 14:

Kaneko teaches the electronic system as rejected in claim 12 above, wherein the third buffer logic provides an indication to an analysis device of the transmission of the test pattern by the second buffer logic to the first buffer logic, and wherein the third buffer logic provides an indication to an analysis device of a signal transmitted by the

first buffer logic in response to the carrying out of a test by the second buffer logic and indicating a status of the test (column 6, lines 10-55).

As per claim 15:

Kaneko teaches the electronic system as rejected in claim 12 above, wherein all three of the first buffer logic, the second buffer logic and the third buffer logic are integrated circuits of substantially similar design, and wherein the interface of the third buffer logic to couple the third buffer logic to an analysis device is of substantially the same design as both a corresponding interface of the first buffer logic to couple the first buffer logic to the first memory array, and a corresponding interface of the second buffer logic to couple the second buffer logic the second memory array (Figures 4A-B).

Claims 1, 16 & 30 are rejected under 35 U.S.C. 102(e) as being unpatentable over Oz et al. US Patent no. 6,771,087 B1.

As per claims 1, 16 & 30:

Oz et al. teaches the test system, buffer logic and method of the claimed invention an electronic system and method comprising: a first memory module having a first memory array (Figure 4 # 101) and a first buffer logic coupled to the first memory array (Figure 4 # 101); and a second memory module having a second memory array (column 6, lines 20-40) and a second buffer logic coupled to the second memory array (Figure 4 # 409), and transmits a test pattern to the first memory module to carry out a test of the first memory module independently of the memory controller (Figure 4 # 400).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Kaneko US Pat no. 5,561,672.

As per claim 8:

Kaneko teaches the electronic system as rejected in claim 6 above, wherein the test pattern is received by the second buffer logic from the test source.

Kaneko discloses the claimed invention except for the test patterns are stored in the buffer and transmitted from the buffer as opposed to the memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made to store the test patterns in the memory and transmit them to the other memory from the first memory, since it has been held that where the general conditions of a claim are

disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 9:

Kaneko teaches the electronic system as rejected in claim 1 above, wherein the test pattern is generated by the second buffer logic in response to commands received by the second buffer logic.

Kaneko discloses the claimed invention except for the test patterns are stored in the buffer and transmitted from the buffer as opposed to the memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made to store the test patterns in the memory and transmit them to the other memory from the first memory, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 11:

Kaneko teaches the electronic system as rejected in claim 10 above.

Kaneko discloses the claimed invention except for the test patterns incorporating a deliberately created error. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a deliberately created error to elicit an expected action, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233. As evidenced by US Pat

no. 5875195 A, injecting errors in test patterns are well known in the art and fall under workable ranges.

As per claims 16-24:

Claims 16-24 are directed to the buffer logic of the system of claims 1-15. Kaneko teaches as stated above, the system as set forth in claims 1-15. Therefore, Kaneko also teaches as stated above, the buffer logic as set forth in claims 16-24.

As per claims 25-29:

Claims 25-29 are directed to performing the method of the system of claims 1-15. Kaneko teaches as stated above, the system as set forth in claims 1-15. Therefore, Kaneko also teaches as stated above, the method as set forth in claims 25-29.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
09/29/2006

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